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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER

KIM, DAVID S

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2613

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/810,203	Applicant(s) KANG ET AL.	
	Examiner DAVID S. KIM	Art Unit 2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 January 2008.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,6,9 and 10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,6,9 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 June 2007 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. In the previous Office Action (Advisory Action mailed on 05 December 2007), there are objections to the drawings. Applicant's most recently filed document is a Request for Continued Examination (RCE) filed on 07 January 2008. This RCE does not include any additional remarks concerning the standing objections to the drawings. Accordingly, Examiner respectfully maintains the previous objections. For detailed reference, here is a copy of the discussion of the drawing objections in the previous Office Action (Advisory Action mailed on 05 December 2007, p. 2, "Drawings" section):

Applicant's response to the objections to the drawings in the previous Office Action (mailed on 28 August 2007) is noted and appreciated. Applicant responded by stating:

"It is asserted in the Office Action that Figures 6-7 include connections that are not supported. Applicant respectfully disagrees.

Applicant notes that on page 6, lines 10-15 of the specification it is asserted that the 'peak value sensor senses the maximum and/or minimum levels from the two outputs.... The error amplifier amplifies a difference between the detected maximum and minimum levels' Therefore, the connections between the peak value sensor and the error amplifier can be sufficiently derived from the foregoing. Approval is respectfully requested" (REMARKS, p. 5).

Examiner respectfully notes that this portion of the specification does not actually define the *number* of connections between the peak value sensor and the error amplifier. Thus, Applicant's response is not persuasive. Accordingly, Examiner respectfully maintains the previous objections.

Claim Objections

2. **Claims 1 and 9** are objected to because of the following informalities:

In claim 1, "a the limiting amplifier" is used where -- a the limiting amplifier -- may be intended (changes shown by Examiner). Otherwise, the usage of "a the" is unclear.

Also, "wherein the differential signal is are output" is used where -- wherein the differential signals is are output -- may be intended (changes shown by Examiner). Otherwise, antecedent basis is inconsistent with the previous instances of plural "differential signals".

Also, "a cascaded set of a plurality of auto-offset cancellation portion" is used where -- ~~a cascaded set of a plurality of an~~ auto-offset cancellation portion -- may be intended (changes shown by Examiner). Otherwise, each "set" of the "series of sets" includes multiple auto-offset cancellation portions, which is in contrast with each set having one auto-offset cancellation portion (see corresponding Fig. 5). Similarly,

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"wherein the auto-offset cancellation portions comprises" is used where -- wherein the auto-offset cancellation ~~portions~~ portion comprises -- may be intended (changes shown by Examiner). Otherwise, the antecedent basis would be unclear.

In claim 9, "a the peak sensor" is used where -- a the peak sensor -- may be intended (changes shown by Examiner). Otherwise, the usage of "a the" is unclear.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 9 and 10** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant amended independent claim 1 to include limitations detailing the "post amplifier", e.g., a "peak value sensor", an "error amplifier", a "limiting amplifier", and an "auto-offset cancellation portion". These limitations correspond to the embodiment of post amplifier 44 in **Fig. 6**. However, dependent claims 9 and 10 include limitations also detailing the "post amplifier", e.g., a "peak value sensor", an "error amplifier", a "first limiting amplifier", an "auto-offset cancellation portion", and a "second limiting amplifier". These limitations of dependent claims 9 and 10 correspond to the embodiment of post amplifier 44 in **Fig. 7**. Since claims 9 and 10 are dependent claims of independent claim 1, the claimed invention of claims 9 and 10 includes a post amplifier that includes limitations of the embodiment of Fig. 6 **and** limitations of the embodiment of Fig. 7. However, Applicant's disclosure does not teach or suggest the use of these two embodiments **together**. Accordingly, dependent claims 9 and 10 introduce subject matter that is **new matter**. As some potential remedies, Examiner respectfully presents the following suggestions:

- Cancel claims 9 and 10.

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- Amend claim 1 so that it is broad enough to correspond to both embodiments of Figs. 6 and 7.
- Amend claim 1 so that it is directed to the embodiment of Fig. 7.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 1, 3, 4, 6, 9, and 10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- In particular, notice the following limitations of independent claim 1:

a peak value sensor which detects the maximum or minimum levels from the outputs of ***a limiting amplifier***; and

an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier,

wherein intrinsic offsets and offsets inherited from a signal output from the differential amplifier are canceled if DC gain from the error amplifier is greater than a DC gain of the limiting amplifier; and ***the post amplifier comprises a series of sets, each of the sets comprising:***

a the limiting amplifier which amplifies the differential signals and cancels offsets inherited from the differential signals or an offset occurring during the amplification according to a predetermined control signal wherein the differential signals is are output from the single-to-differential converter for the first set and output from the limiting amplifier of the previous set for the subsequent sets; and

a cascaded set of a plurality of auto-offset cancellation portion which calculates a difference between outputs of the limiting amplifier, amplifies the difference, and provides the amplification result as the predetermined control signal to the limiting amplifier, wherein the auto-offset cancellation portions comprises:

the peak value sensor; and

the error amplifier.

(emphasis Examiner's).

Notice the initial introduction of "***a peak value sensor***", "***an error amplifier***", and "***a limiting amplifier***". Later in the claim, there is the "***post amplifier***", which "***comprises a series of sets***".

Each of these sets comprises "***the peak value sensor***", "***the error amplifier***", and "***a the limiting amplifier***". However, notice, again, that the initial introduction of "***a peak value sensor***", "***an error amplifier***", and "***a limiting amplifier***" only introduces *one* instance of each of these claim elements. The "***series of sets***" implies multiple instances of "***the peak value sensor***", "***the error amplifier***", and "***a the limiting amplifier***", i.e., one instance of each of these elements for each set. Thus, the following questions arise about the scope of the claim:

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Is there **only one** instance of each of these claim elements?

If so, how can each set comprise **the same one** instance of each of these claim elements?

If not, why does the claim introduce **only one** instance of each of these claim elements?

These questions indicate that the language of claim 1 (and its dependent claims) is **indefinite**.

As a remedy, Examiner respectfully suggests the following changes to the language of claim 1:

~~a peak value sensor which detects the maximum or minimum levels from the outputs of a limiting amplifier; and~~

~~an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier;~~

~~wherein intrinsic offsets and offsets inherited from a signal output from the differential amplifier are canceled if DC gain from the error amplifier is greater than a DC gain of the limiting amplifier; and the post amplifier comprises a series of sets, each of the sets comprising:~~

~~a the limiting amplifier which amplifies the differential signals and cancels offsets inherited from the differential signals or an offset occurring during the amplification according to a predetermined control signal wherein the differential signals is are output from the single-to-differential converter for the first set and output from the limiting amplifier of the previous set for the subsequent sets; and~~

~~a cascaded set of a plurality of an auto-offset cancellation portion which calculates a difference between outputs of the limiting amplifier, amplifies the difference, and provides the amplification result as the predetermined control signal to the limiting amplifier, wherein the auto-offset cancellation portions portion comprises:~~

~~the a peak value sensor which detects the maximum or minimum levels from the outputs of the limiting amplifier; and~~

~~the an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier,~~

~~wherein intrinsic offsets and offsets inherited from a signal output from the differential amplifier are canceled if DC gain of the error amplifiers is greater than the DC gain of the limiting amplifiers.~~

7. **Claims 9 and 10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Similar to the discussion of independent claim 1 above (35 U.S.C. 112, second paragraph), claim 9 introduces similar issues. In particular, notice the following limitations of claim 9:

(from parent claim 1)

a peak value sensor which detects the maximum or minimum levels from the outputs of a limiting amplifier; and

an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier,

(from claim 9)

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The burst mode optical receiver of claim 1, wherein ***the post amplifier comprises cascaded sets, each of the sets comprising:***

a first limiting amplifier which amplifies the differential signals and cancels the offsets inherited from the differential signals or the offset occurring during the amplification according to the predetermined control signal;

an auto offset cancellation portion which calculates a difference between the outputs of the first limiting amplifier, amplifies the difference, and provides the amplification result as the predetermined control signal to the first limiting amplifier;

a second limiting amplifier which amplifies differential signals output from the first limiting amplifier; and

wherein the differential signals is-are output from the single-to-differential converter for the first set and output from the second limiting amplifier of the previous set for the subsequent sets, and the auto-offset cancellation portion comprises:

a the peak value sensor which detects the maximum and minimum levels from the outputs of the first limiting amplifier; and

the error amplifier.

Similar to the discussion of independent claim 1 above, notice the initial introduction of "***a peak value sensor***" and "***an error amplifier***" in parent claim 1. Later in claim 9, there is the "***post amplifier***", which "***comprises cascaded sets***". Each of these sets comprises "***a the peak value sensor***" and "***the error amplifier***". However, notice, again, that the initial introduction of "***a peak value sensor***" and "***an error amplifier***" only introduces ***one*** instance of each of these claim elements. The "***cascaded sets***" implies multiple instances of "***the peak value sensor***" and "***the error amplifier***", i.e., one instance of each of these elements for each set. Thus, the following questions arise about the scope of the claim:

Is there ***only one*** instance of each of these claim elements?

If so, how can each set comprise ***the same one*** instance of each of these claim elements?

If not, why does the claim introduce ***only one*** instance of each of these claim elements?

These questions indicate that the language of claim 9 (and its dependent claim 10) is ***indefinite***.

As a remedy, Examiner respectfully suggests the following changes to the language of claims 1 and

9:

(from parent claim 1)

~~a peak value sensor which detects the maximum or minimum levels from the outputs of a limiting amplifier; and~~

~~an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier;~~

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(from claim 9)

The burst mode optical receiver of claim 1, wherein the post amplifier comprises cascaded sets, each of the sets comprising:

a first limiting amplifier which amplifies the differential signals and cancels the offsets inherited from the differential signals or the offset occurring during the amplification according to the predetermined control signal;

an auto offset cancellation portion which calculates a difference between the outputs of the first limiting amplifier, amplifies the difference, and provides the amplification result as the predetermined control signal to the first limiting amplifier;

a second limiting amplifier which amplifies differential signals output from the first limiting amplifier; and

wherein the differential signals are output from the single-to-differential converter for the first set and output from the second limiting amplifier of the previous set for the subsequent sets, and the auto-offset cancellation portion comprises:

a the peak value sensor which detects the maximum and minimum levels from the outputs of the first limiting amplifier; and

the an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the first limiting amplifier.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. **Claims 1 and 3-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono (U.S. Patent Application Publication No. US 2002/0109075 A1) in view of Ide et al. (U.S. Patent No. 5,955,921, hereinafter "Ide") and Hatakeyama et al. (U.S. Patent No. 6,018,407, hereinafter "Hatakeyama").

Regarding claim 1, Ono discloses:

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A burst mode optical receiver (e.g., Fig. 41) comprising:

a photodiode which converts an input optical signal into a current signal (PD);

a pre-amplifier which converts the current signal into a voltage signal (IV);

a single-to-differential converter which converts the single voltage signal output from the pre-amplifier into differential signals (AMP);

a post amplifier which amplifies the differential signals and cancels an offset occurring during the amplification or offsets inherited from the differential signals (DAMP and VOS); and

a discriminator which discriminates data from the differential signals (CMP).

Ono does not expressly disclose:

a single-to-differential converter which converts the single voltage signal output from the pre-amplifier into differential signals wherein the single-to-differential converter comprises a differential amplifier which receives a predetermined reference voltage as a first input and the single voltage signal as a second input to output symmetrical differential signals.

However, such a structure is known in the art, as shown by the automatic threshold control (ATC) circuit of Ide (Fig. 30). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include an ATC circuit in the single-to-differential converter of Ono. One of ordinary skill in the art would have been motivated to do this to provide a wide dynamic range (Ide, col. 2, l. 25-26), which enables the receiver of Ono to follow variations in the level of the input signal (Ide, col. 2, l. 20-24).

Ono in view of Ide does not expressly disclose (but Hatakeyama does):

a peak value sensor which detects the maximum or minimum levels from the outputs of a limiting amplifier (e.g., PD(1)P or PD(1)N in Fig. 7); and

an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier (e.g., AMP(1) in Fig. 7).

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wherein the post amplifier comprises a series of sets (e.g., amplifiers after PRE in Fig. 7), each of the sets comprising:

a limiting amplifier (e.g., LIM(1)) which amplifies the differential signals and cancels offsets inherited from the differential signals or an offset occurring during the amplification (col. 1, l. 1. 48-51) according to a predetermined control signal (e.g., signals from AMP(1)) wherein the differential signals are output from the single-to-differential converter for the first set and output from the limiting amplifier of the previous set for the subsequent sets; and

an auto-offset cancellation portion (e.g., loopback components in LIM(1)) which calculates a difference between outputs of the limiting amplifier, amplifies the difference, and provides the amplification result as the predetermined control signal to the limiting amplifier, wherein the auto-offset cancellation portion comprises:

the peak value sensor; and

the error amplifier.

However, such a structure is known in the art, as shown by the offset compensating amplifying circuits of Hatakeyama (e.g., amplifiers after PRE in Fig. 7). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to such offset compensating teachings in the post amplifier of Ono in view of Ide. One of ordinary skill in the art would have been motivated to do this since doing so would compensate (Hatakeyama, col. 1, l. 1. 48-51) the offset from differential amplifiers/signals, such as the differential amplifier(s)/signals of Ono (Ono, DAMP in Fig. 41) in view of Ide.

Ono in view of Ide and Hatakeyama does not expressly disclose:

wherein intrinsic offsets and offsets inherited from a signal output from the differential amplifier are canceled if DC gain from the error amplifier is greater than a DC gain of the limiting amplifier.

However, notice that this limitation is an **intended result, not a particular structure** of the claimed apparatus. Claim scope is not limited by claim language that suggests or makes optional but does

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not limit a claim to a particular structure (See MPEP 2111.04). Since this claim is an apparatus claim, it must be **structurally distinguishable** from the prior art (See MPEP 2114). Moreover, the manner of operating Applicant's claimed apparatus does not differentiate it from the prior art if the prior art apparatus teaches all of the **structural** limitations of the claim (See MPEP 2114). Therefore, since this limitation does not structurally distinguish Applicant's claimed invention from the prior art of record, this limitation does not limit the scope of the claim. Accordingly, this limitation does not patentably distinguish Applicant's claimed invention from the prior art of record.

Moreover, notice that this intended result is credited to the structure of Applicant's Fig. 6. Next, notice the similarities between the structure of Applicant's Fig. 6 (more details on p. 6, l. 3-22) and the structure of the prior art of record (Hatakeyama, Fig. 7, col. 1, l. 47 – col. 2, l. 9). In some ways, they seem even identical. Since the claimed intended result is credited to the structure of Applicant's Fig. 6, one would expect similar, if not identical, results from the similar, if not identical, structure of the prior art of record.

Regarding claim 3, Ono in view of Ide and Hatakeyama discloses:

The burst mode optical receiver of claim 2, wherein the single-to-differential converter further comprises an auto threshold controller (Ide, 102 in Fig. 30) which detects maximum and minimum levels (Ide, peak and bottom detecting circuits) of the single voltage signal and provides a substantial middle value of the maximum and minimum levels as a first input to the differential amplifier (Ide, "intermediate value" in col. 2, l. 4-9).

Regarding claim 4, Ono in view of Ide and Hatakeyama discloses:

The burst mode optical receiver of claim 3, wherein the auto threshold controller comprises:

- a top holder which detects the maximum level of the single voltage signal and holds the maximum level for a predetermined period of time (Ide, peak detecting circuit in Fig. 30);
- a bottom holder which detects the minimum level of the single voltage signal and holds the minimum level for a predetermined period of time (Ide, bottom detecting circuit in Fig. 30); and
- a voltage divider which detects the substantial middle value of the maximum and the minimum levels (Ide, voltage dividing circuit in Fig. 30).

Regarding claim 6, Ono in view of Ide and Hatakeyama discloses:

The burst mode optical receiver of claim 1, wherein the limiting amplifier is a differential amplifier (Hatakeyama, notice the positive-phase and negative-phase output signals from limiter amplifiers LIM) that operates in a linear region (amplifiers commonly operate in a linear region).

Regarding claim 9, Ono in view of Ide and Hatakeyama discloses:

The burst mode optical receiver of claim 1, wherein the post amplifier comprises cascaded sets, each of the sets comprising:

a first limiting amplifier (e.g., Hatakeyama, LIM(1) in Fig. 7) which amplifies the differential signals output from the single-to-differential converter and cancels the offsets inherited from the differential signals or the offset occurring during the amplification according to the predetermined control signal (Hatakeyama, offset compensation in LIM(1));

an auto offset cancellation portion (e.g., Hatakeyama, PD(1)P and PD(1)N and AMP(1) and summers in Fig. 7) which calculates a difference between the outputs of the first limiting amplifier, amplifies the difference (Hatakeyama, AMP(1)), and provides the amplification result as the predetermined control signal to the first limiting amplifier (Hatakeyama, summers); and

a second limiting amplifier (e.g., Hatakeyama, LIM(2)) which amplifies differential signals output from the first limiting amplifier; and

wherein the differential signal is output from the single-to-differential converter for the first set (LIM(1) of Fig. 7 of Hatakeyama after AMP of Fig. 41 of Ono) and output from the second limiting amplifier of the previous set for the subsequent sets (e.g., LIM(3) of Fig. 7 of Hatakeyama after LIM(2) of Fig. 7 of Hatakeyama), and the auto-offset cancellation portion comprises:

a the peak value sensor which detects the maximum and minimum levels from the output of the first limiting amplifier (e.g., Hatakeyama, PD(1)P or PD(1)N in Fig. 7); and

the error amplifier (e.g., Hatakeyama, AMP(1) in Fig. 7).

Regarding claim 10, Ono in view of Ide and Hatakeyama discloses:

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The burst mode optical receiver of claim 9, wherein the first or second limiting amplifier is a differential amplifier (Hatakeyama, notice the positive-phase and negative-phase output signals from limiter amplifiers LIM) that operates in a linear region (amplifiers commonly operate in a linear region).

Response to Arguments

11. Applicant's arguments filed 07 January 2008 have been fully considered but they are not persuasive. Applicant's most recently filed document is a Request for Continued Examination (RCE) filed on 07 January 2008. This RCE does not include any additional remarks concerning the standing rejections of the claims. However, the RCE does include the following remark: "Consider the arguments in the Response filed on June 8, 2007" (RCE Transmittal form, item 1.a.ii.). Examiner already considered these arguments and concluded that they were not persuasive (see the Final Rejection mailed on 28 August 2007, p. 8-9).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hirose et al. ("An ultracompact, 2-cc-size, low-power 2.5-Gb/s optical receiver module incorporating an MU receptacle") is cited to show a post amplifier comprising a series of sets, each of the sets comprising a limiting amplifier and an auto-offset cancellation portion (Fig. 8).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID S. KIM whose telephone number is (571)272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. S. K./
Examiner, Art Unit 2613


KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER